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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,011	07/03/2002	Gilbert Wolrich	10559-312US1	5760

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,011	WOLRICH ET AL.	
	Examiner	Art Unit	
	William M. Treat	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-36 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-36 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. Applicants claim in claim 1 and its dependent claims 2-29 (and have similar language in claims 30-36): "directing the processor having a plurality of threads executing in a plurality of microengines to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting". Applicants state on page 3 of their specification that "The micro engines 22a-22f can execute memory reference instructions to either the SDRAM controller 26a or SRAM controller 16b." Also, on page 3 applicants state: "The SRAM controller 26b controls arbitration for the SRAM bus, accesses the SRAM 16b, fetches the data from the SRAM 16b, and returns data to a requesting micro engine 22a-22f. During an SRAM access, if the micro engine, e.g., micro engine 22a had only a single thread that could operate, that micro engine would be dormant until data was returned from the SRAM 16b. By employing hardware context swapping within each of the micro engines 22a-22f the hardware context swapping enables other contexts with unique

program counters to execute in that same micro engine. Thus, another thread, e.g.. Thread_1 can function while the first thread, i.e., Thread_0, is awaiting the read data to return." In other words, applicants' specification teaches issuing the memory reference instruction of a thread to an address in a memory shared among threads executing in the microengines while the context of thread is **active** and then **inactivating** the thread **(i.e., place the thread in a wait state)**. **The memory reference instruction of the thread is not issued while the thread is waiting as applicants are claiming, and there is no enablement for such a claim in applicants' specification.**

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. See paragraph 4, *supra*, for a relevant explanation of the deficiency.

8. Claims 1-23, 26, and 30-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwal et al. (APRIL: A Processor Architecture for Multiprocessing).

9. The reasons set forth in the examiner's previous actions for rejecting claims 1-23, 26, and 30-36, as being anticipated by Agarwal, continue and are hereby incorporated by reference.

10. Applicants argue on behalf of claims 1-23, 26, and 30-36, in substance, that (a) Agarwal teaches much that applicants do not teach, and (b) Agarwal does not teach "directing the processor having a plurality of threads executing in a plurality of

microengines to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting."

11. As to 10(a), the examiner would remind applicants that it is important that the reference teach applicants' **claimed** invention and it is irrelevant that the reference teaches additional matters. The reference could teach it has an engine with dual carburetors that supply power for its system but that would be irrelevant if applicants made no claim to their source of power for their system.

12. As to 10(b), applicants have argued on behalf of independent claims 1 and 30 and their dependent claims that Agarwal does not teach "directing the processor having a plurality of threads executing in a plurality of microengines to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting" or similar language. As noted in paragraph 4, *supra*, the examiner does not think even applicants disclosed what is claimed. However, if applicants are merely claiming a microengine/microprocessor can issue such a memory reference for a thread while some other thread on some other microprocessor is inactive, Agarwal certainly taught that (pp. 104-106, Sections 2 and 3 in their entirety). Agarwal states: "APRIL is the processing element of ALEWIFE, a large-scale multiprocessor being designed a MIT. ALEWIFE is a cache-coherent machine with distributed, globally-shared memory." (Section 2, first sentence) He also states: "As shown in Figure 1, each ALEWIFE node consists of a processing element, floating-point unit, cache, main memory, cache/directory controller, and a network routing switch." And, "On exception conditions such as cache misses and failed

synchronization attempts, the controller can choose to trap the processor or make the processor wait." (Section 2.1) At the top of page 107, Agarwal further states: "APRIL continues executing a single thread until a memory operation involving a remote request (or an unsuccessful synchronization attempt) is encountered." Note that Agarwal describes a multiple node processor with each node containing a microprocessor/microengine based on Sun Microsystem's SPARC processor, with each SPARC processor capable of supporting four hardware contexts/threads, and with threads capable of making memory requests to the distributed, globally-shared memory in Sections 2, 2.1, 2.2, 3, 3.1, 3.2, 3.3, and 3.4. In Section 4 under the title "Memory Instructions" Agarwal describes the memory instructions used by his microprocessor/microengine that will result in the cache/directory controller of his microprocessor/microengine continuing to execute the memory access to the shared memory while the relevant context has been swapped out and is waiting. Agarwal has a memory controller which continues access to the shared memory while the swapped out thread waits just as applicants' system does. Applicants' language of independent claim 1, **supported by their original disclosure**, fails to distinguish over the prior art of record as does the language of independent claim 30.

13. Note that applicants' retreat into vague verbiage, such as microengine for what was originally claimed as microprocessor, does not provide patentable differentiation for applicants' claims.

14. Also, applicants' misunderstanding of the fact that the context swap occurs when the SPARC microprocessor thread cannot find the memory reference in the local portion

of shared memory, and the memory controller must then access more remote shared memory (see paragraph 12, *supra*) does not impart patentability to their claims. Applicants mistakenly thought the context swap was predicated on one microprocessor trying to access a second microprocessor's local portion of shared memory causing the second microprocessor's active thread to swap out.

15. As a further point the examiner would note, applicant also misunderstood the problem Agarwal's system addressed. Agarwal taught how to continue to do useful work in a system by using multithreading in multiple processors and by swapping out threads which were awaiting the results of shared memory accesses so that other threads could do useful work. This is no different from applicants' goals.

16. Finally, **though not claimed**, applicants seem to imply in their arguments using known fabrication technology to create on a chip a system that mimics Agarwal's basic design might provide patentable differentiation. Copying and miniaturizing someones basic design is not invention.

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claims 24-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (APRIL: A Processor Architecture for Multiprocessing).

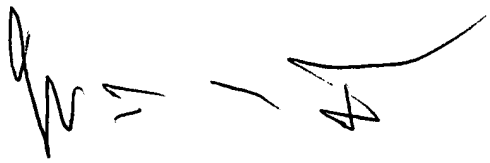
20. The reasons set forth in the examiner's previous actions for rejecting claims 24-25 and 27-29 continue and are hereby incorporated by reference.

21. As to applicants' arguments on behalf of claims 24-25 and 27-29, see paragraphs 10-16, *supra*.

22. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may normally be reached in the afternoon and evening on three of the four remaining weekdays.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER